AMENDMENTS TO THE DRAWINGS:

Figures 1-8 are identified as prior art.

REMARKS

The application has been amended and is believed to be in condition for allowance.

Responsive to the drawing objection, prior art legends have been added to Figures 1-8.

New claims are added and are based on the disclosure discussed below and illustrated by Figures 9-10. These claims correspond to elected Group I.

There are no other formal matters outstanding.

Claims 1-8 stand rejected as obvious over the Application's Disclosed Prior Art (APA) Figures 1-8 in view of NISHIO 6,160,275.

In order to compare the invention to the prior art, a review of the Application's Disclosed Prior Art would be helpful.

FIG.5

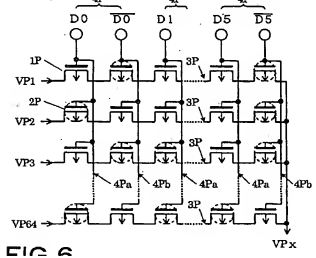
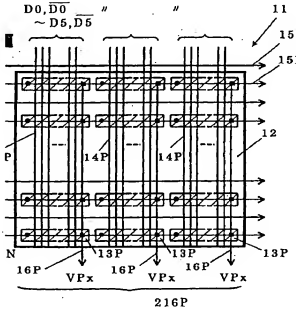


FIG.6



As per specification page 12, Figure 5 is a circuit diagram of one stage of P-ROM decoder 216P contained in the circuit block of Figure 4, and Figure 7 includes a schematic diagram showing a plan pattern on the semiconductor chip of the P-ROM decoder 216P contained in the circuit block of Fig. 4. These are reproduced above.

As discussed on specification pages 13-18, Figure 5 shows that the P-ROM decoder 216P includes pairs of P-channel enhancement type transistors 1P and P-channel depletion type transistors 2P (kept under ON-state at all times) are arranged at predetermined positions side-by-side at the pair of confronting gate wires. One gates of the respective pairs of transistors on the respective rows are commonly connected to one another every column to thereby form gate array 4Pa, and the other gates of the respective pairs of transistors on the respective rows are commonly connected to one another every column to thereby form gate array 4Pb so that each gate array 4Pa and each gate array 4Pb constitute gate array pair 4P.

The pattern arrangement of the P-ROM decoder 216P is shown as in Figure 7. The P-ROM decoder 216P is designed so that three stages of P-type diffusion layers 13P serving as the sources and drains of the transistors 1P, 2P arranged in a matrix of 64 rows × 12 columns, and three stages of gate wires 14P serving as six pairs of gate array pairs 4P are contained in an

N-well 12 arranged on the P-type semiconductor substrate 11. The P-type diffusion layers 13P serving as the sources of the respective first-column transistors 1P and 2P are electrically commonly connected to one another by metal wires 15P every line (shown by symbol •). The P-type diffusion layers 13P serving as the drains of the respective twelfth transistors 1P and 2P are electrically commonly connected to one another through metal wires 16P every column (shown by symbol ■).

Figure 8 (below) is a diagram showing a pattern arrangement of gate wires of one stage of the P-ROM decoder of Figure 7. Figure 9 corresponds to one embodiment of the present invention.

FIG.8

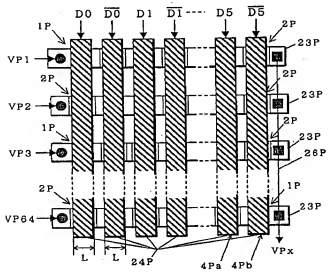
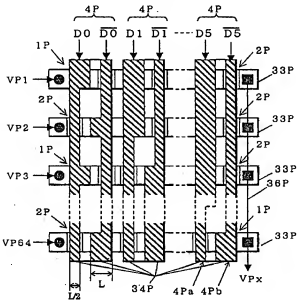


FIG.9



That the prior art, as shown in Figure 8, gate wires 24P having a uniform wire width of L (for example, L = 2 μm) and an interval S between gate wires (for example, S = 1 μm).

Contrast the uniform wire width of the prior art to the pattern arrangement of the gate wires 14P of the P-ROM decoder 216P as an example with reference to Fig. 9.

In the gate wires 34P, the width of the gate wire that contains the upper portion of the depletion type transistor 2P (kept under ON-state at all times) and extends from the depletion type transistor 2P to the two adjacent enhancement type transistors 1P is set to a half of the gate wire width L so that recess portions are formed at the insides of the confronting gate wires 34P of the respective gate array pairs 4P. With reference to Figure 10, the width of the gate wire that contains the upper portion of the depletion type transistor 2P is set to a half of the gate wire width L so that recess portions are formed at the insides of the confronting gate wires 34P of the respective gate array pairs 4P.

Therefore, in each embodiment, with respect to each of the pair of the confronting gate wires 34P, the width of the gate wire between continuously-arranged depletion type transistors 2P is reduced thanks to recess portions formed inside the confronting gate wires.

In the invention, the enhancement type transistors 1P have a gate wire width of L and the depletion type transistors 2P have a gate wire width of L/2. Thus, the overall width of two adjacent transistors is 2L in the invention as opposed to 2½L in the prior art of Figure 8.

However, in the invention, the dimension concerned is not limited to these values, and it may be set to any value which is smaller than L and within a range in which it functions as a conductive wire. Accordingly, the layout dimension of the arrangement of both the gate wires in the chip longitudinal direction can be reduced and also the gate wire area can be reduced by the narrowed amount of the gate wire width. Therefore, there can be provided a liquid crystal driving semiconductor integrated circuit device in which the layout area of the ROM decoder and the gate capacity can be reduced.

In a nutshell, Figures 9-10 show that in the invention, the width of the gate wire that contains the upper portion of the depletion type transistor is narrower than the width of the gate wire than contains the upper portion of the adjacent enhancement type transistor. This provides that recess portions are formed inside the confronting gate wires. Claim 1 has been amended to make this more specific.

Turning now to the pending claims, claim 1 recites that the pairs each comprise an enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires. This is shown by the prior art Figure 8. Claim 1 further requires that the width of the gate wire that contains the upper portion of the depletion type transistor is

narrower than the width of the gate wire than contains the upper portion of the adjacent enhancement type transistor.

NISHIO does not make is disclosure.

NISHIO makes no disclosure concerning the width of gate wire between two adjacent transistors be different.

NISHIO makes no disclosure concerning the width of the gae wire being narrower for depletion type transistors than for the enhancement type transistors.

NISHIO makes no disclosure that would provide recess portions formed inside the confronting gate wires.

NISHIO discloses that to save space one kind "down size" individual transistors so that two transistors can be used to meet the requirement of one transistor. Under such a teaching, there would be no reason to vary the width of the gate wire between adjacent transistors.

NISHIO therefore does not teach the invention as claimed.

Further, NISHIO's teaching is not relevant to the present invention, in particular to Figures 1-8 as this design does not have pairs of transistors that can be used together to "down size" as taught by NISHIO.

As to claim 2, see the embodiment of Figure 10, wherein wherein the width of the gate wire for the depletion type transistor extends from the depletion type transistor to the position between the depletion type transistor and the adjacent

enhancement type transistor such that that reduced recess portions are formed inside the confronting gate wires.

Again, NISHIO does not make is disclosure as NISHIO makes no disclosure concerning the width of gate wire between two adjacent transistors be different, and NISHIO makes no disclosure that would provide recess portions formed inside the confronting gate wires.

NISHIO therefore does not teach the invention as claimed in claim 2.

The Official Action does not seem to have addressed claims 3-6. These claims are also not taught by either prior art Figures 1-8 or NISHIO. See for example, claims 5-6 which recite wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor. There is no teaching in NISHIO to have the gate wire of a first transistor type be half the width of the gate wire at another transistor type.

Thus, NISHIO would not render obvious these dependent claims.

As to the new claims, NISHIO does not teach anything that would suggest modifying Figures 1-8 so that the recited invention results.

NISHIO does not teach anything that would suggest modifying Figures 1-8 so that a gate wire has a first width over the depletion type transistor and a second width over an adjacent

enhancement type transistor, the first width being less than the second width such at a recess is formed in the gate wire between two enhancement type transistors.

NISHIO does not teach the first width of the gate wire over the depletion type transistor is equal to a half of the second width of the gate wire over the enhancement type transistor.

NISHIO does not teach an overall width of the pair of confronting gate wires is twice the second width.

Thus, the new claims are believed patentable.

Reconsideration and allowance of all the claims are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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APPENDIX:

- Replacement sheets for Figures 1-8